DESCRIPTION

Preliminary Specification

The NN518128 is a high performance CMOS Dynamic Random Access Memory organized as 131,072 words by 8 bits. The NN518128 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN518128 features a high speed page mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

The outputs are tri-stated by $\overline{CAS}$ which, in essence, acts as an output enable independent of $\overline{RAS}$ with very fast CAS to output access time.

Refresh is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A0 to A8 during a 8 ms period.

Multiplexed address inputs permit the NN518128 to be packaged in a standard 26-pin plastic SOJ. The package sizes provide high system bit densities. System level features include single power supply of 5V ±10% tolerance and direct interface with high performance TTL logic families.

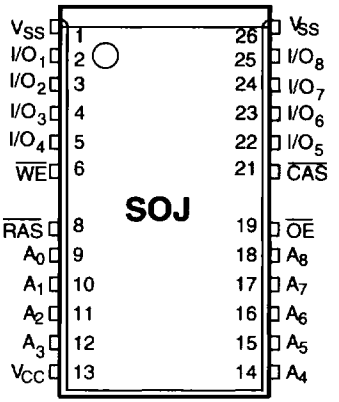
FEATURES

- 131,072 × 8 bit Organization
- Single 5V ±10% Power Supply
- Performance Ranges

Parameter	-50	-60	-70
Max. $\overline{RAS}$ Access Time (t_{RAC})	50ns	60ns	70ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	15ns	15ns	20ns
Max. Column Address Access Time (t_{AA})	25ns	30ns	35ns
Min. Read/Write Cycle Time (t_{RC})	90ns	110ns	130ns

- Fast Page Mode Operation
- Low Power Operation
  Low Standby Current (CMOS level input)
  – Standard 1mA
  – L version 50μA
- 512 Refresh Cycles
  – Standard distributed across 8ms
  – L version distributed across 32ms
- Self Refresh Mode
  (L version)
- All inputs/Outputs and Clocks
  fully TTL and CMOS compatible
- Refresh Modes
  $\overline{RAS}$ only
  $\overline{CAS}$ before $\overline{RAS}$
  Hidden Refresh
- High Reliability Packages
  Plastic 26pin SOJ (P26SJ-2A2)

PIN CONFIGURATION

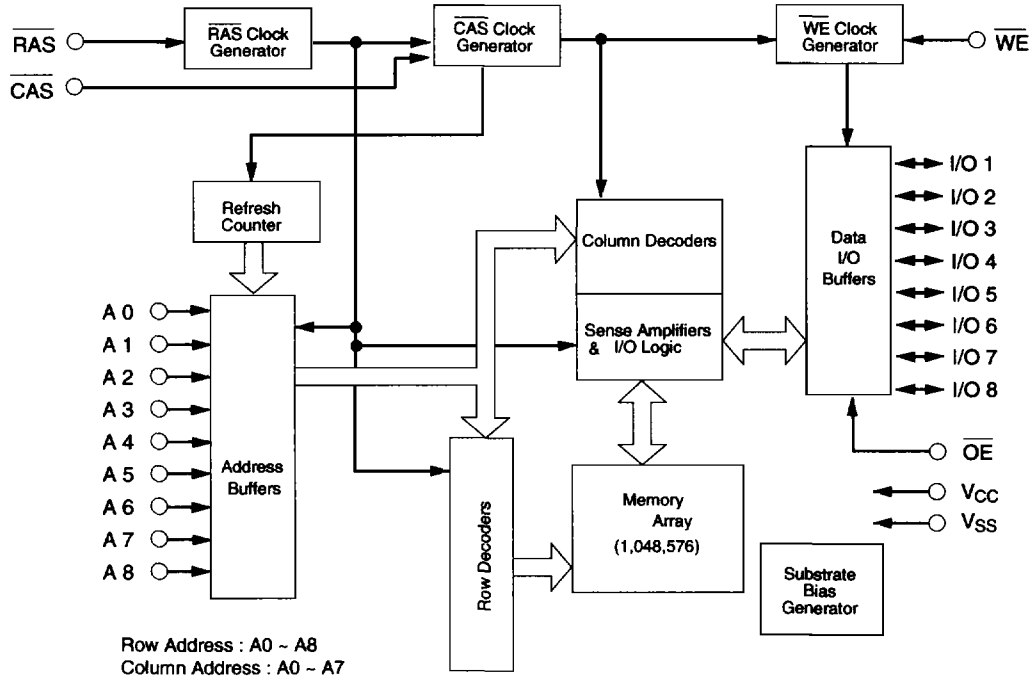


26-pin SOJ (300mil)
P26SJ-2A2

PIN NAMES

A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{OE}$	Output Enable
I/O1~I/O8	Data-in / Data-out
$\overline{WE}$	Write Enable
V_{CC}	+5V Supply
V_{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	Vin,Vout	−1 to 7	V
Voltage on Vcc Relative to V_{SS}	V_{CC}	−1 to 7	V
Storage Temperature (Plastic)	Tstg	−55 to +125	°C
Power Dissipation	Pd	1.0	W
Ambient Operating Temperature	Ta	0 to + 70	°C
Short Circuit Output Current	Iout	50	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage, All Inputs	2.4	—	6.5	V
V_{IL}	Input Low Voltage, All Inputs	−1.0	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I_{CC1}	Operating Current	-50 -60 -70		100 90 80	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$, Address cycling	1, 2
I_{CC2}	Standby Current			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V)	
				2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}	
	Standby Current (L version)			50	µA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC3}	Refresh Current ($\overline{RAS}$ only refresh)	-50 -60 -70		100 90 80	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}	1
I_{CC4}	Fast Page Mode Current	-50 -60 -70		70 60 50	mA mA mA	t_{PC} = t_{PC} (min.) $\overline{RAS}$ = V_{IL} $\overline{CAS}$, Address cycling	1,2
I_{CC5}	Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	-50 -60 -70		100 90 80	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$ cycling	1
I_{CC6}	Refresh Current (L version : $\overline{CAS}$ before $\overline{RAS}$ refresh)			150	µA	512 cycles / 32ms t_{RAS} ≤ 200ns, $\overline{WE}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC7}	Self Refresh Mode Current (L version)			100	µA	RAS = CAS ≤ (V_{SS} + 0.2V) All other inputs high levels are (V_{CC} - 0.2V) or input low levels are (V_{SS} + 0.2V)	
$\|I_{L1}\|$	Input Leakage Current (Any input pin)		-10	10	µA	0V ≤ V_{IH} ≤ 5.5V, Others = 0V	
$\|I_{LO}\|$	Output Leakage Current (For high impedance state)		-10	10	µA	$\overline{RAS}$ ≥ V_{IH} (min.), $\overline{CAS}$ ≥ V_{IH} (min.) 0V ≤ V_{OUT} ≤ 5.5V	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = –5.0 mA	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	

Notes: 1. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Address(A0 ~ A8)	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,$\overline{OE}$	—	5	pF
C_{OUT}	I/O1 ~ I/O8	—	7	pF

A.C. OPERATING CONDITIONS (0 °C≤Ta≤70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (NOTES 3, 4, 5)

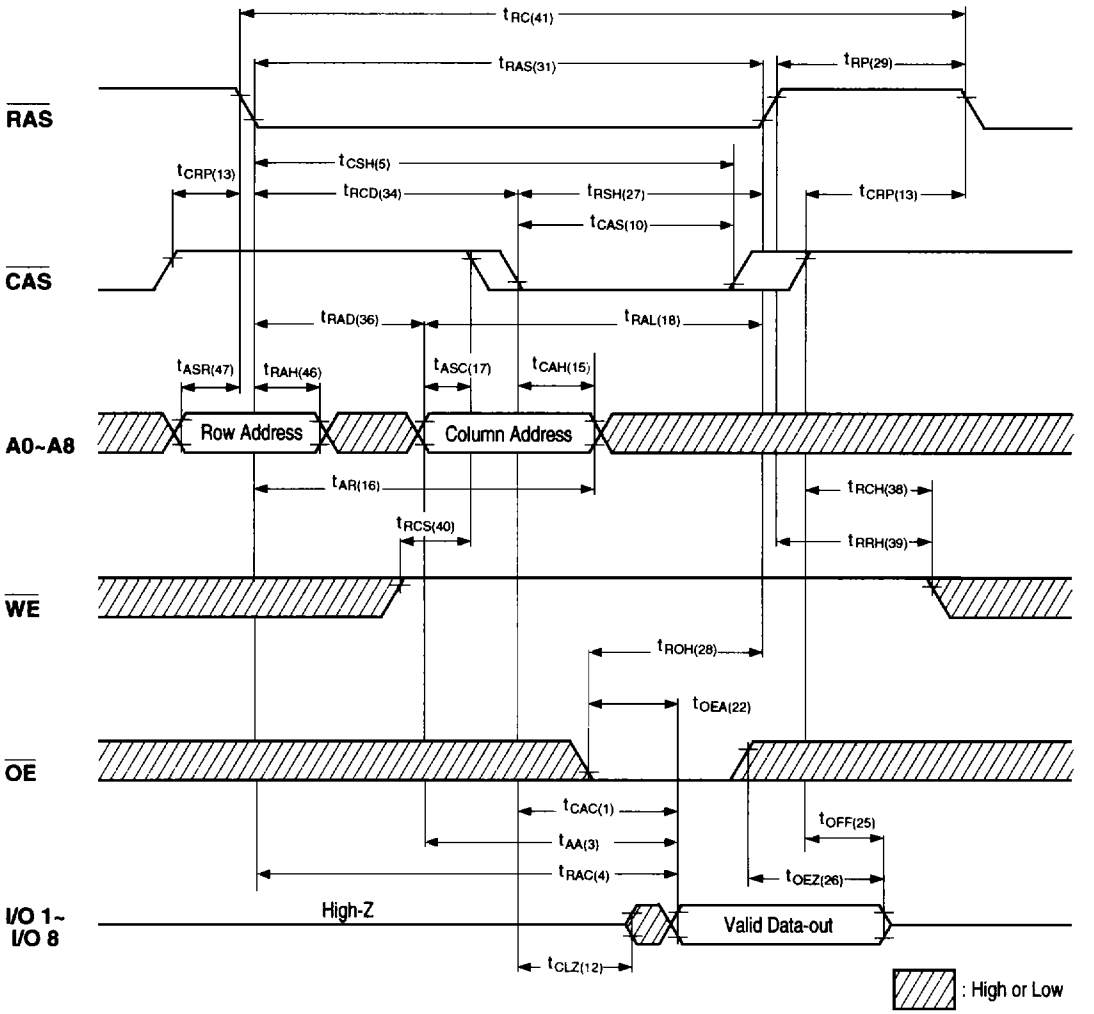
NO.	SYMBOL		PARAMETER	-50		-60		-70		UNIT	NOTE
	JEDEC	STD		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	15	—	20	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	35	—	40	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	25	—	30	—	35	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	60	—	70	ns	6,7
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	50	—	60	—	70	—	ns	
6	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	ns	
7	t_{RL1CX}	t_{CHS}	$\overline{CAS}$ Precharge Time (Self Refresh Mode)	-50	—	-50	—	-50	—	ns	
8	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	15	100K	15	100K	20	100K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	45	—	50	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10	—	15	—	15	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	35	—	40	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	14
18	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	27	—	30	—	35	—	ns	
19	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	57	—	60	—	65	—	ns	11
20	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	10	—	10	—	15	—	ns	12
21	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	ns	12
22	t_{OL1QV}	t_{OEA}	$\overline{OE}$ Access Time	—	15	—	15	—	20	ns	
23	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	15	—	20	—	ns	
24	t_{CH2QV}	t_{OED}	$\overline{OE}$ to Data Delay Time	10	—	10	—	10	—	ns	
25	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	13	0	15	0	20	ns	10
26	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{OE}$	0	10	0	15	0	15	ns	
27	t_{CL1RH1}	t_{RSH}	$\overline{RAS}$ Hold Time	15	—	15	—	20	—	ns	
28	t_{OL1RH1}	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	—	10	—	10	—	ns	
29	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	25	—	30	—	40	—	ns	
30	t_{RH2RL2}	t_{RPS}	$\overline{RAS}$ Precharge Time (Self Refresh Mode)	90	—	110	—	130	—	ns	
31	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	50	100K	60	100K	70	100K	ns	
32	t_{RL1RH1}	t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	50	100K	60	100K	70	100K	ns	
33	t_{RL1RH1}	t_{RASS}	$\overline{RAS}$ Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	µs	
34	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	13	35	13	45	13	50	ns	6
35	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
36	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	11	23	11	30	11	35	ns	7
37	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	—	90	—	100	—	ns	11
38	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	9
39	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	10	—	10	—	10	—	ns	9

NO.	SYMBOL		PARAMETER	-50		-60		-70		UNIT	NOTE
	JEDEC	STD		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
40	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	9
41	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	90	—	110	—	130	—	ns	
42	t_{CL2CL2}	t_{PC}	Read or Write Cycle Time (Fast Page Mode)	33	—	40	—	45	—	ns	13,14
43	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	145	—	165	—	185	—	ns	
44	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (Fast Page Mode)	90	—	95	—	100	—	ns	13,14
45	t_{REF}	t_{REF}	Refresh Period	—	8	—	8	—	8	ms	15
46	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8	—	8	—	8	—	ns	
47	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
48	t_T	t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	4,5
49	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10	—	10	—	15	—	ns	
50	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	10	—	10	—	15	—	ns	
51	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	ns	11
52	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	15	—	20	—	ns	
53	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	15	—	20	—	ns	

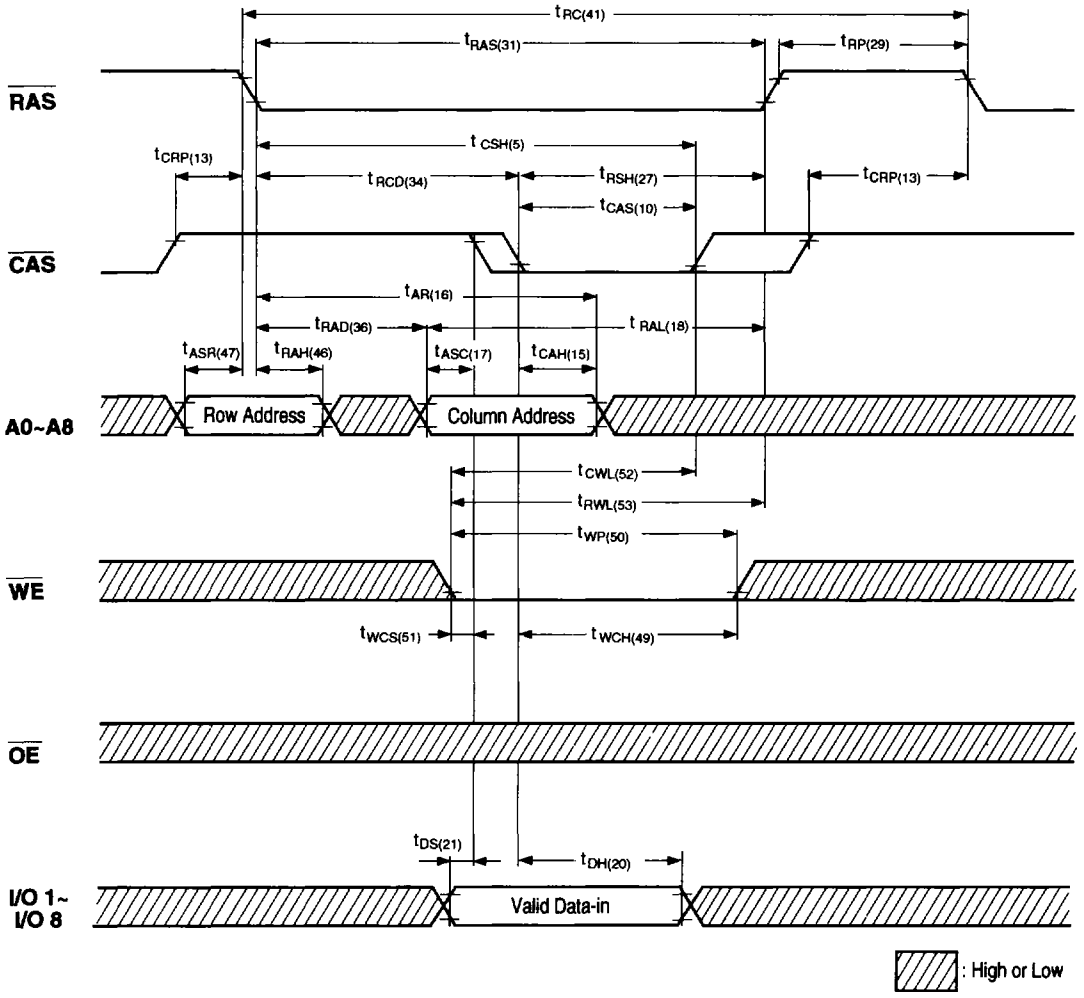
Notes:

3. Eight Initialization Cycles are required following a 200μs pause after Power Up.
   These Initialization Cycles may consist of any combination of the following : $\overline{RAS}$ only refresh Cycles, Read Cycles, Write Cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh Cycles.
4. AC measurements assume t_T=3ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC} and with a load equivalent to two TTL loads and 50pF.
5. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
7. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
8. Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF}(max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS}≥t_{WCS}(min.) , the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If t_{RWD}≥t_{RWD}(min.), t_{CWD}≥t_{CWD}(min.) and t_{AWD}≥t_{AWD}(min.), the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
14. t_{ASC}≥t_{CP} to achieve t_{PC}(min.) and t_{CPA}(max.) values.
15. t_{REF}=32 msec for Long Refresh version (L version)

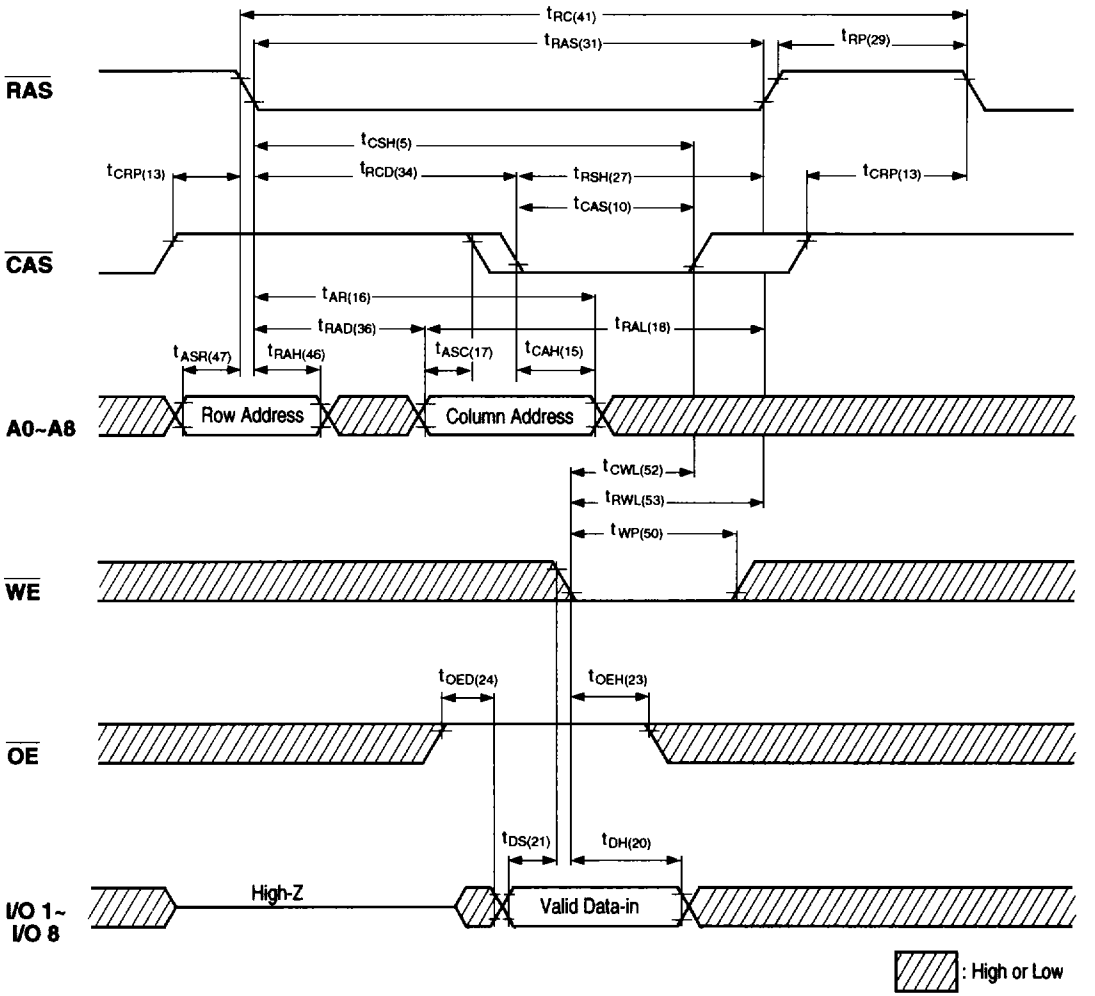
READ CYCLE


tRC(41)
tRAS(31)
tRP(29)
RAS
tCSH(5)
tCRP(13)
tRCD(34)
tRSH(27)
tCRP(13)
tCAS(10)
CAS
tRAD(36)
tRAL(18)
tASR(47)
tRAH(46)
tASC(17)
tCAH(15)
A0~A8
Row Address
Column Address
tAR(16)
tRCH(38)
tRCS(40)
tRRH(39)
WE
tROH(28)
tOEA(22)
OE
tCAC(1)
tOFF(25)
tAA(3)
tRAC(4)
tOEZ(26)
I/O 1~
I/O 8
High-Z
Valid Data-out
tCLZ(12)
: High or Low

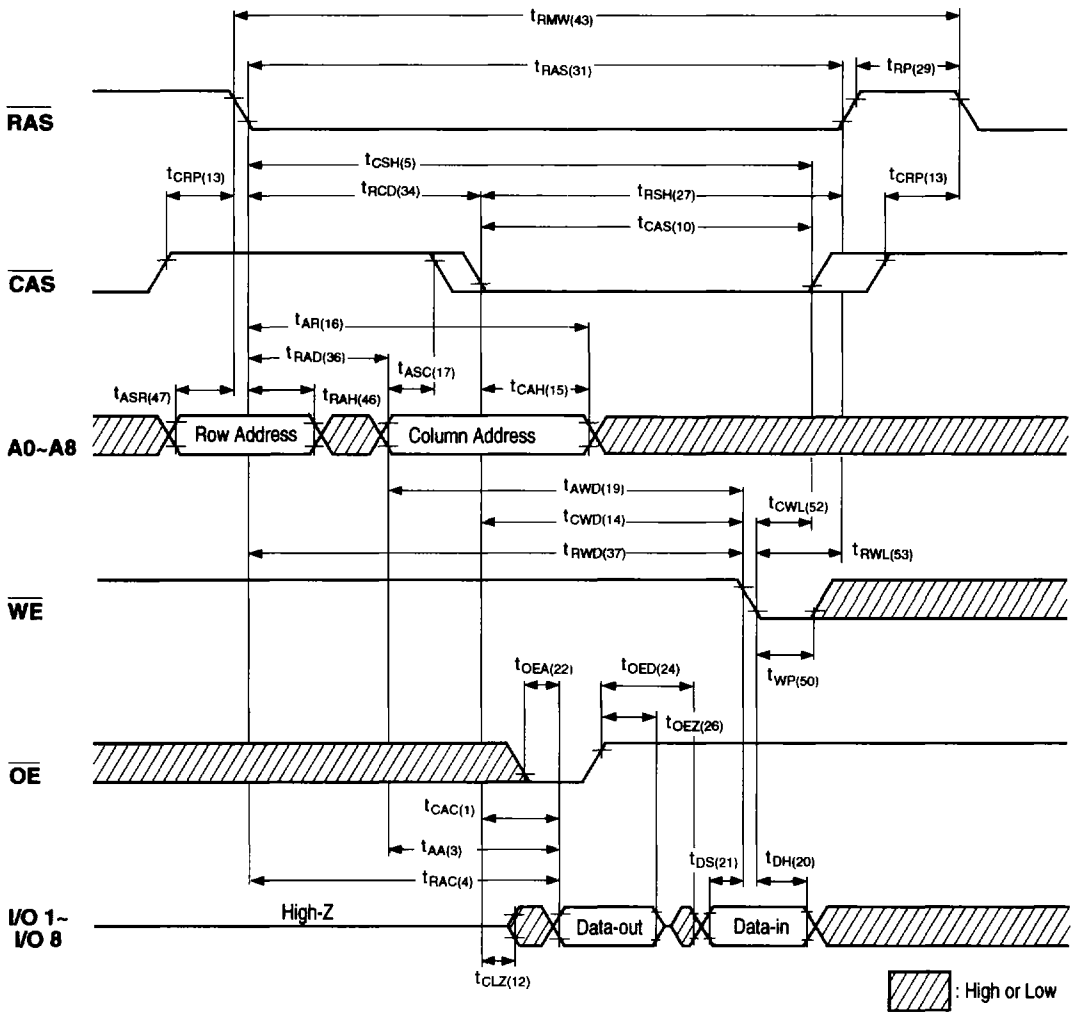
WRITE CYCLE (EARLY WRITE)



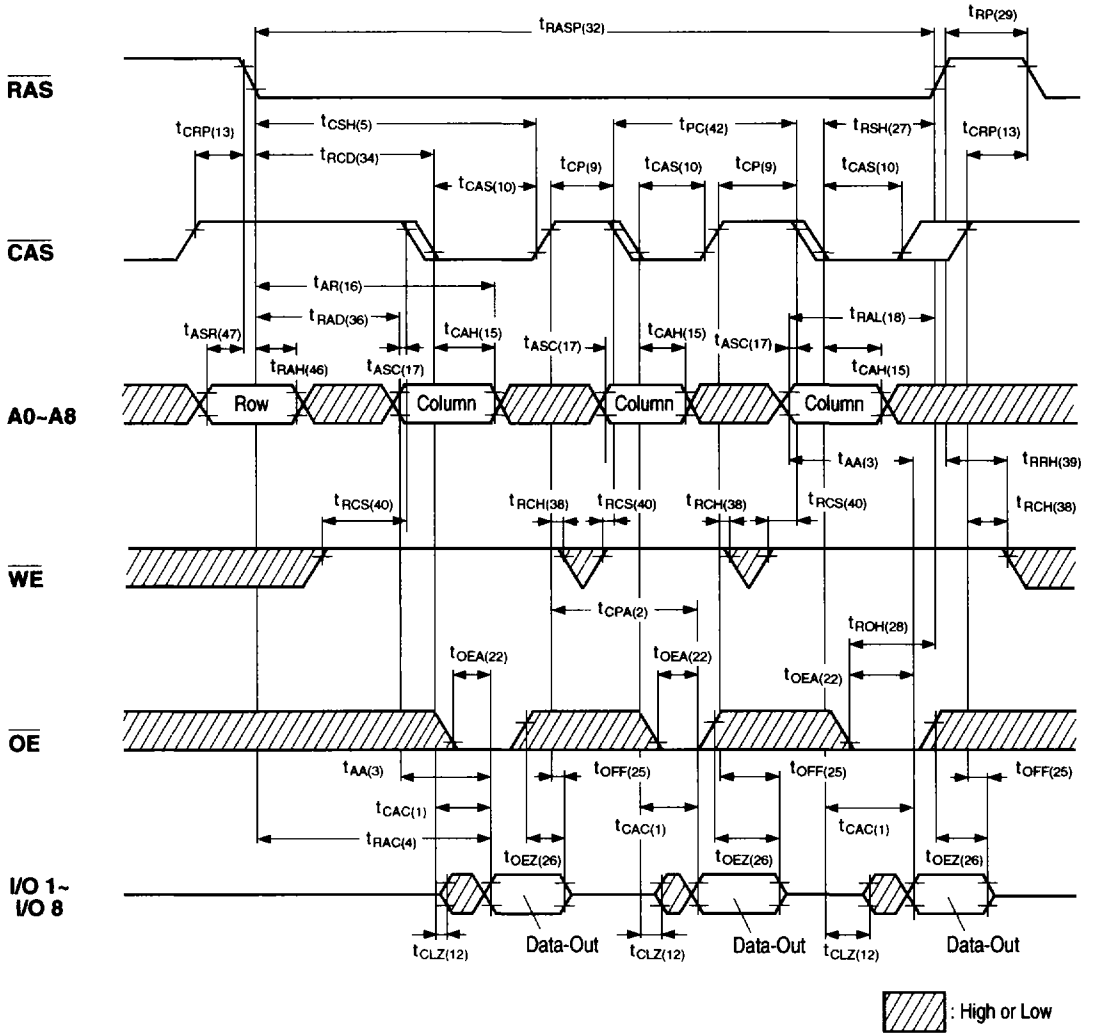
WRITE CYCLE (OE-CONTROLLED WRITE)



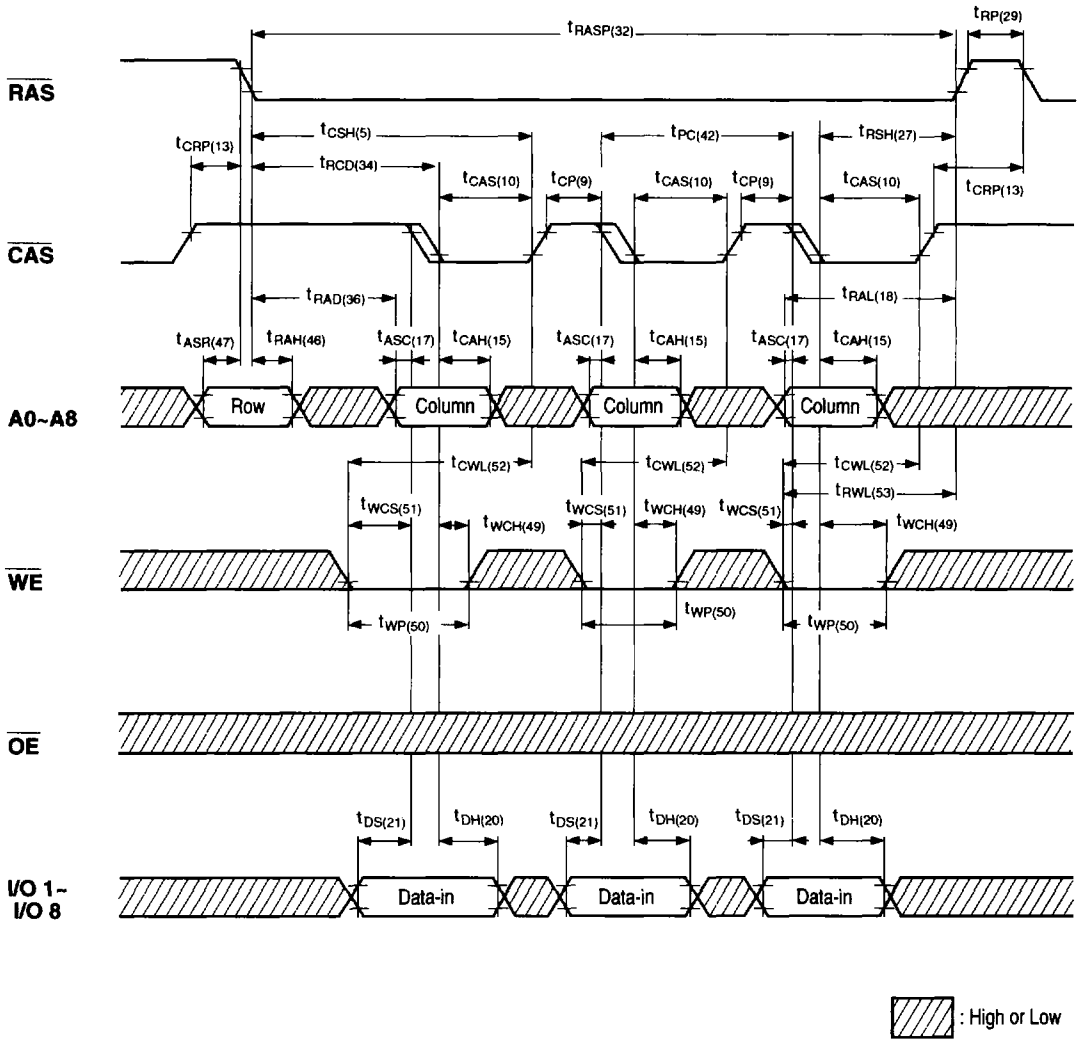
READ-MODIFY-WRITE CYCLE



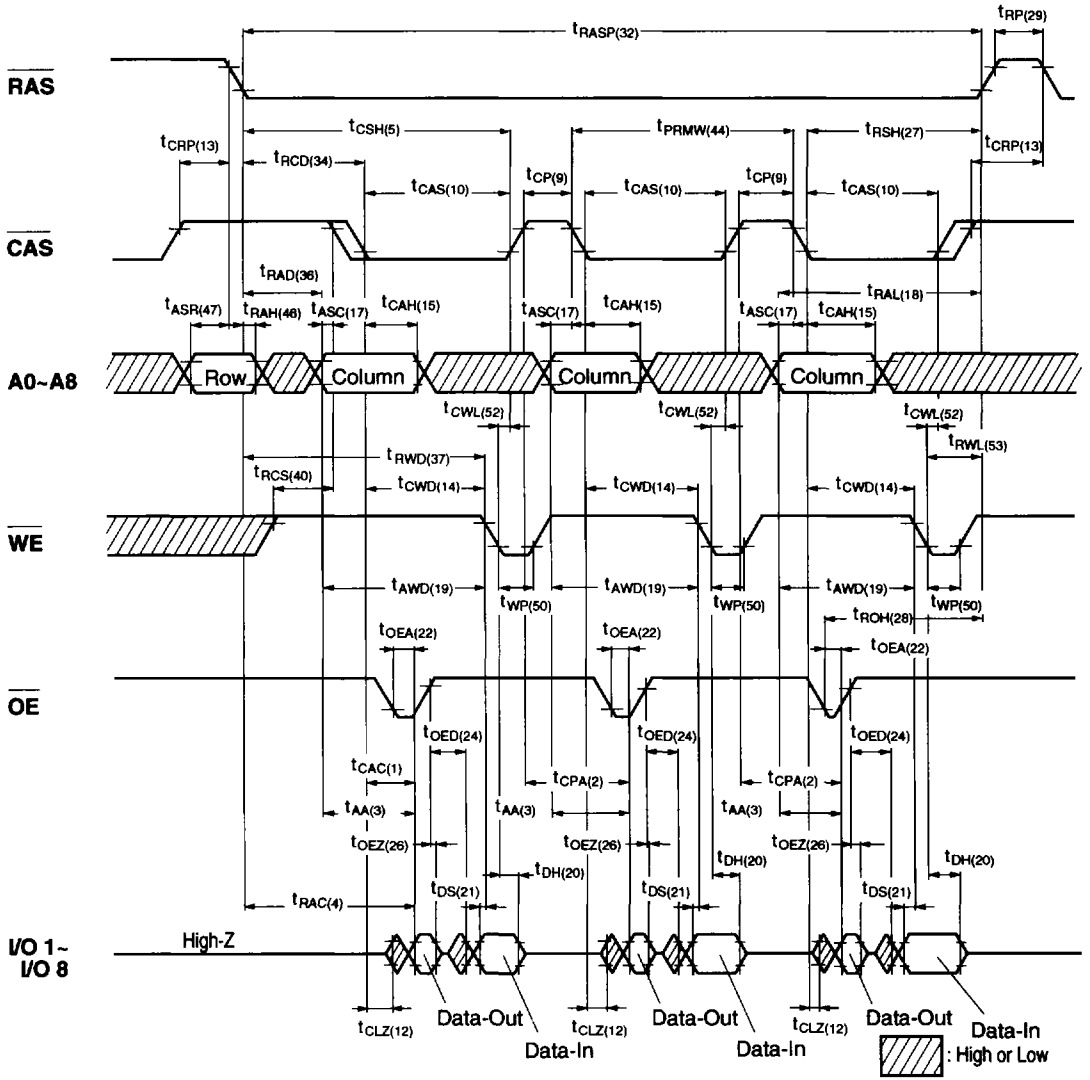
FAST PAGE MODE READ CYCLE



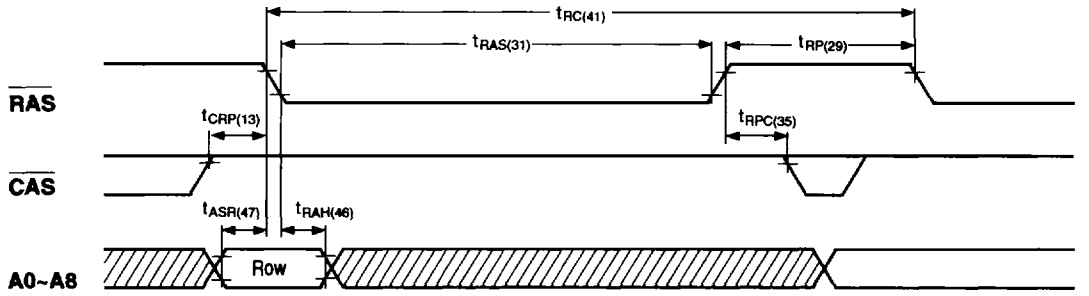
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



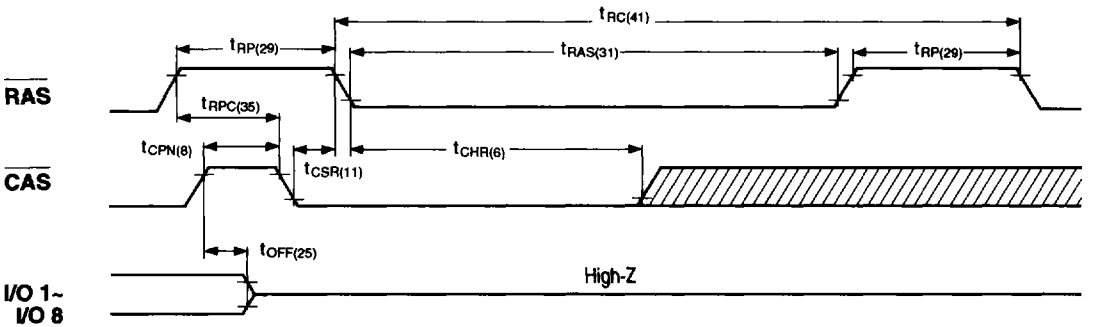
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

: High or Low

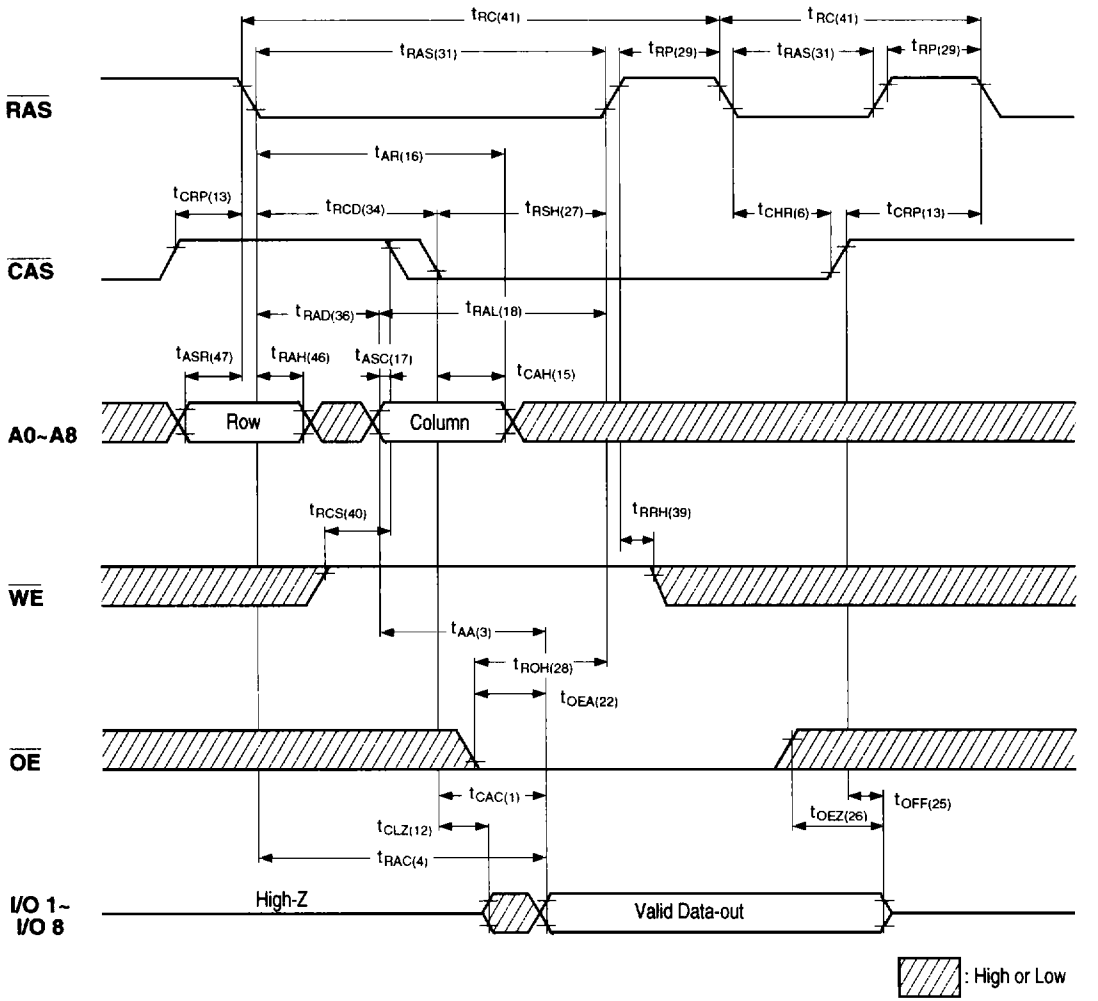
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



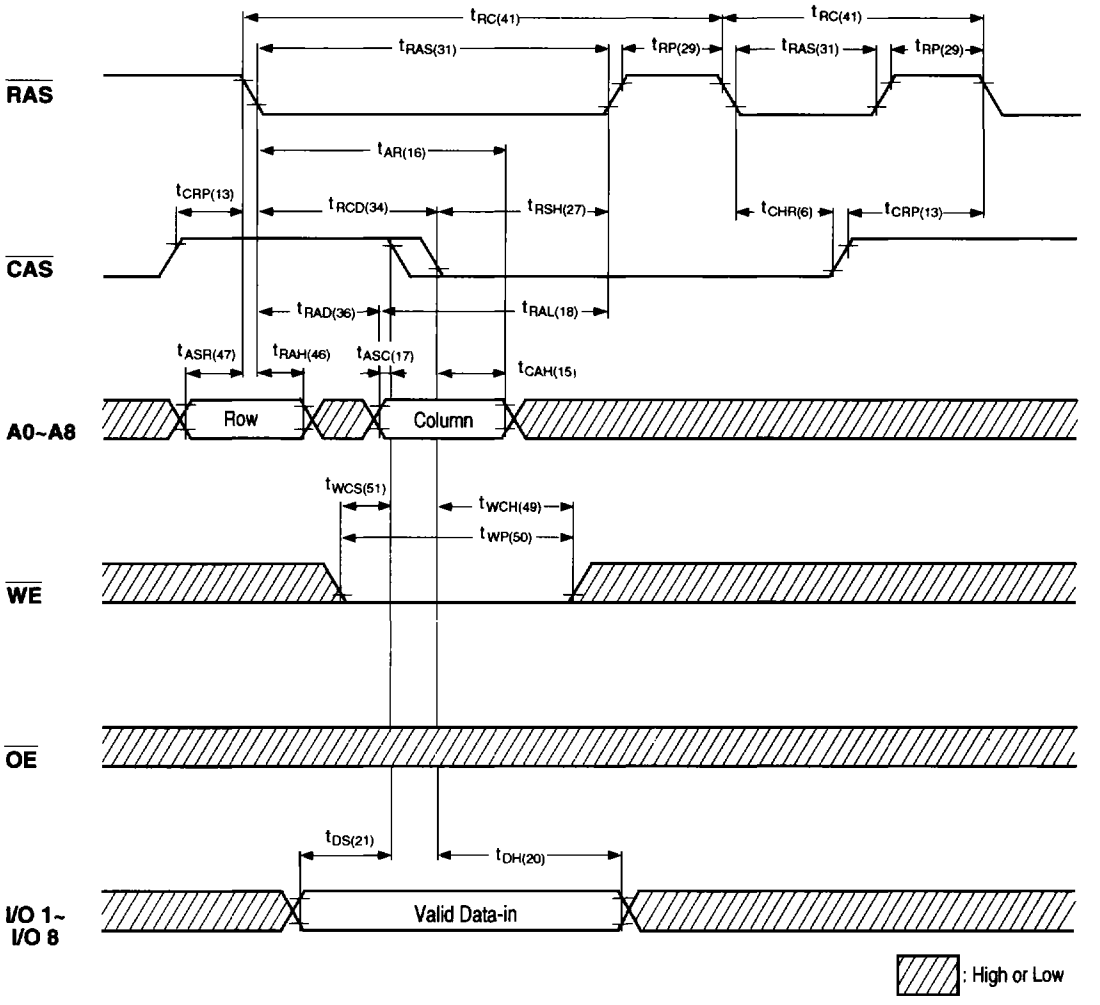
Note: $\overline{WE}$, $\overline{OE}$, A0~A8 = Don't care.

: High or Low

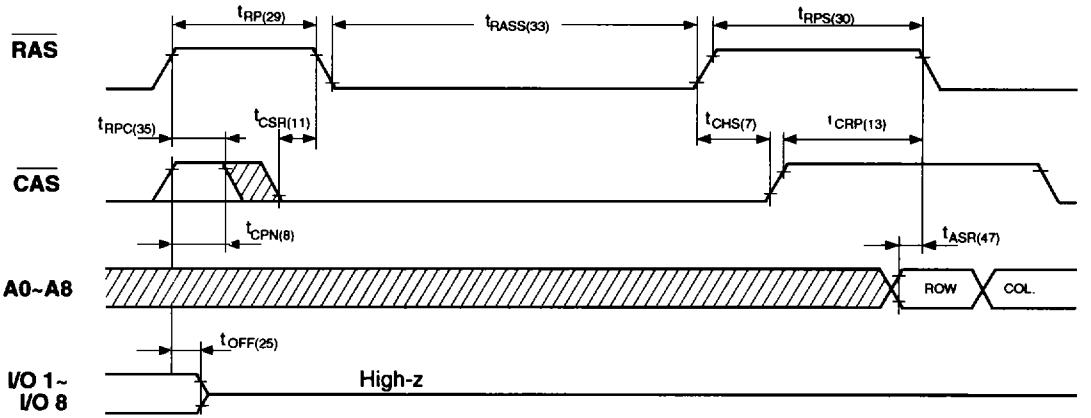
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



SELF REFRESH MODE



■ The NN518128L has a Self Refresh Mode.

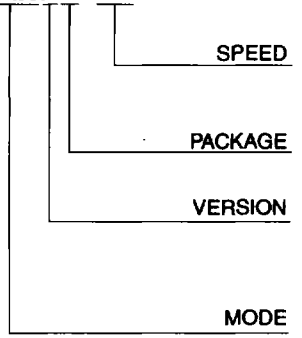
a. Entering the Self Refresh Mode:
The NN518128L Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle and holding $\overline{RAS}$ and $\overline{CAS}$ signal " low " longer than 300μs.

b. Continuing the Self Refresh Mode:
The Self Refresh Mode is continued by holding $\overline{RAS}$ " low " after entering the Self Refresh Mode.
It does not depend on being $\overline{CAS}$ " high " or " low " after entering the Self Refresh Mode to continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:
The NN518128L exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought " high ".

ORDERING INFORMATION

NN518128XJ - XX



SPEED	50	:	50ns
	60	:	60ns
	70	:	70ns
PACKAGE	J	:	Plastic SOJ
VERSION	BLANK	:	Standard Version
	L	:	Long Refresh Version 32ms Refresh
MODE	8128	:	Fast Page 128K x 8 512 refresh Cycle